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K-Band Via-Hole Grounding π-Gate FET with Monolithic On-Chip Matching Network*

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ABSTRACT

A 1650 μm gate width GaAs FET with monolithic partial on-chip matching network of the input for broadband operation had 630 mW output power with 4 dB gain from 17 to 20.5 GHz. The π-gate design includes 13 reactive-ion-etched source vias on a 50 μm substrate with a plated heat sink.

We have designed, fabricated and tested a 1650 μm gate width FET which includes several state-of-the-art features: it is of the π-gate configuration for best performance at K-band - very low source lead inductance is achieved through via holes under each of the 13 source pads - very low thermal impedance is offered by the 50 μm (2 mils) thick substrate with integral plated heat-sink - partial impedance matching of the input is achieved on the chip with a simple series L shunt C network for operations from 17 to 21 GHz.

This circuit brings the low input impedance of the FET to a nominal 12.5 Ω for broadband matching. This eliminates the need to rely on a discrete L-C-L lumped element matching network where the critical inductance from the gate to the capacitor is provided by bond wires.

Figure 1(a) is a photograph of the FET. The chip size is 2 x 1.4 mm^2 (80 x 54 $mils^2$). A large bonding pad on the 50 μm thick substrate is used to provide a 1 pF capacitance to ground. Twelve 5 μm wide and 1 mm long microstrip line connect each gate feed to the bonding pad.

The front surface processing is conventional. The Ti/Pt/Au 0.5 μm gate is defined by e-beam machine in the 3 μm wide source-drain spacing. The microstrip lines and bonding pads are gold plated to a 3 μm thickness. The wafer is ground to 6 mils, mounted on a sapphire disk and thinned down to 50 μm by rotary etch. Alignment of the 50 x 50 μm^2 holes is done with an IR tower and Reactive Ion Etching is used to achieve high aspect ratio of the vias. Ti/Au is evaporated and 50 μm thick gold is plated on the heat-sink. The devices are finally sawed. Figure 1(b) shows the back surface of a chip with the clearly visible 13 source vias.

The chip was mounted in a circuit for microwave testing. The wide input bonding pad was connected to a 25 Ω quarter-wave transformer by a mesh and bond wires were used on the drain side. Figure 2 shows a photograph of the mounted chip. Figure 3 shows that the return loss is better than 10 dB from 17 to 20.5 GHz with no tuning done. When narrow band tuning was performed on the drain side, the device was capable of 1 W output power at 17 GHz with 5 dB gain and 18% power added efficiency. With the output tuned for broadband operation, 630 mW was achieved with 4 dB gain from 17 to 20.5 GHz. Figure 4 shows the gain response of the device with 24 dBm input power from 17 to 21 GHz.

In conclusion we have demonstrated a 1650 μm gate width device which includes several key features for optimum operation at K-band: on-chip matching of the input, π-gate configuration, via holes in 50 μm thick substrate under each source pad. Both narrow band and wide band operation were demonstrated.

ACKNOWLEDGEMENT

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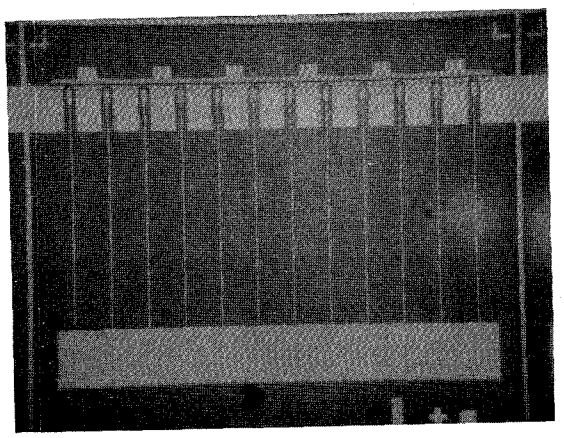

Figure 1(a). 1650 μm FET
Front Surface

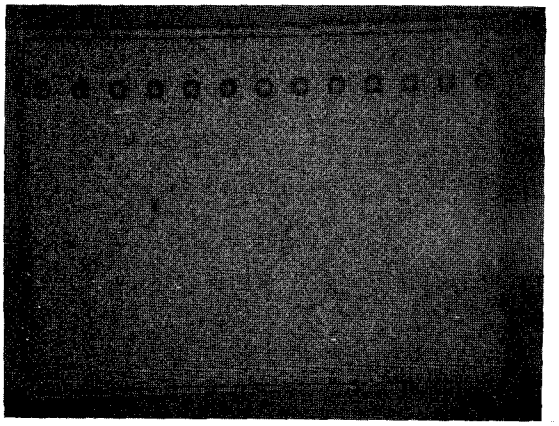

Figure 1(b). 1650 μm
Back Surface

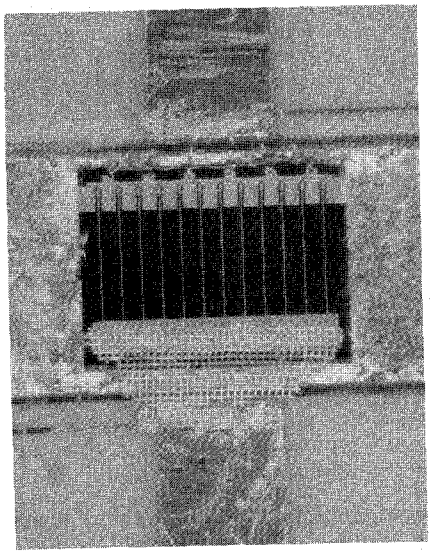

Figure 2. 1650 μm FET Bonded
in Microwave Circuit

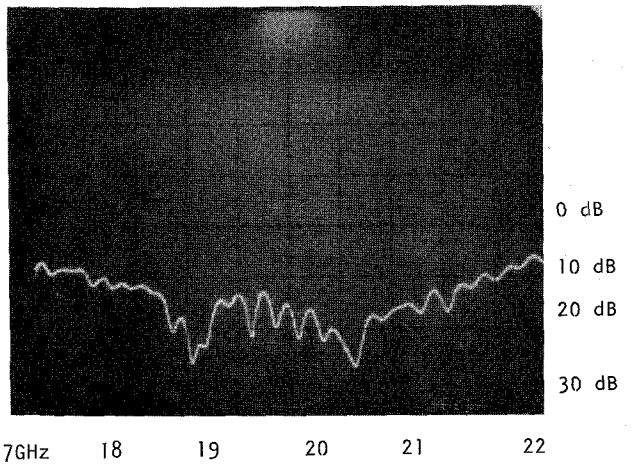

Figure 3. Return Loss
Horizontal 500 MHz/div
Vertical 10 dB/div

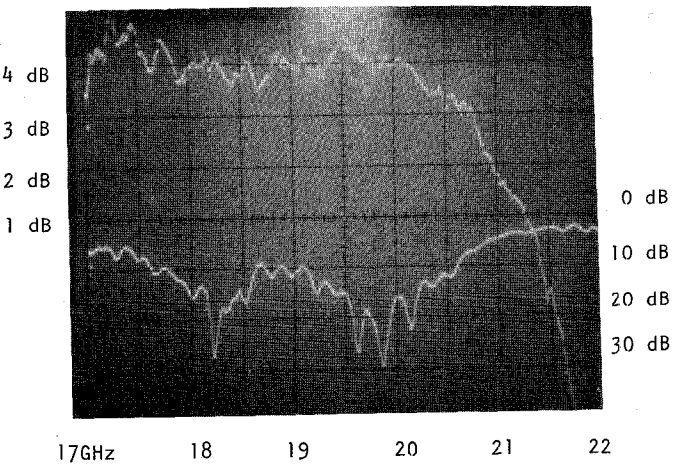

Figure 4. FET Frequency Response
Input Power 24 dBm
Upper Trace: Gain 1 dB/div
Lower Trace: Return Loss
10 dB/div